

**REMARKS**

Claims 1-6 are pending. By this Amendment, claims 3, 5 and 6 are amended for clarification purposes only, and not to distinguish over the prior art. Reconsideration is respectfully requested.

It is gratefully appreciated that the Office Action indicates that claims 3 and 4 contain allowable subject matter.

The Office Action objects to Fig. 1 for not including reference number 19. Fig. 1 is amended to include reference number 19. Thus, withdrawal of the objection is respectfully requested.

The Office Action objects to claim 3 because of an informality. Claim 3 is amended to correct the informality. Thus, withdrawal of the objection of claim 3 is respectfully requested.

The Office Action rejects claims 3-6 under 35 U.S.C. §112, second paragraph. Claims 3, 5 and 6 are amended to obviate the rejection. Thus, withdrawal of the rejection is respectfully requested.

The Office Action rejects claims 1, 5 and 6 under 35 U.S.C. §102(b) over Warren (U.S. Patent No. 5,946,344); and claim 2 under 35 U.S.C. §103(a) over Warren and Ovens (U.S. Patent No. 5,381,455). The rejections are respectfully traversed.

In particular, the applied references do not disclose or suggest at least that an output of each output stage of a shift register is multiplied by a filter coefficient and added, as recited in independent claims 1 and 2.

Specifically, the Office Action asserts that Fig. 2 in Warren discloses an n-stage shift register 12 in which the output of each stage is multiplied by  $2^{2M}$  by a filter coefficient (M) and added by an adder 24. However, Warren instead discloses that the exclusive OR logic gates 22 and 32 "compare" the signals contained in respective delay stages 14<sub>K</sub>-14<sub>L</sub> to the

corresponding chips of first and second spreading codes M and N, respectively. See col. 4, lines 33-36. The summing devices 24 and 34 then sum the outputs of the exclusive OR logic gates 22 and 32 to provide a sum value that is proportional to a degree of correlation between the received signal and first and second spreading codes MN, respectively. In fact, the structure shown in Fig. 2 of Warren in which a received signal is input to one shift register, and a reference code is input to another shift register, is completely different from the structure of the claimed invention. Specifically, the structure in Warren does not receive data that is input to both divided shift registers.

Ovens discloses an interleaved shift register 20 that includes a plurality of data storage elements 22a-22d having a common data input signal.

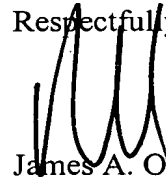
In contrast to the claimed invention, the applied references do not disclose or suggest at least an output of each output stage of a shift register being multiplied by a filter coefficient and added. On the contrary, nowhere in the applied references are these features disclosed or suggested.

Thus, Warren fails to disclose each and every feature as a claimed invention. Moreover, because Ovens fails to compensate for deficiencies in Warren, it is respectfully requested that the rejections under 35 U.S.C. §102(b) and 35 U.S.C. §103(a) be withdrawn.

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1-6 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,



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JAO:RSE/djb

Attachment:  
Replacement Sheet

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<p><b>DEPOSIT ACCOUNT USE AUTHORIZATION</b> Please grant any extension necessary for entry; Charge any fee due to our Deposit Account No. 15-0461</p>
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**Amendments to the Drawings:**

The attached replacement drawing sheet makes changes to Fig. 1 and replaces the original sheet with Fig. 1.

Attachment: Replacement Sheet